

FIGURE 1A

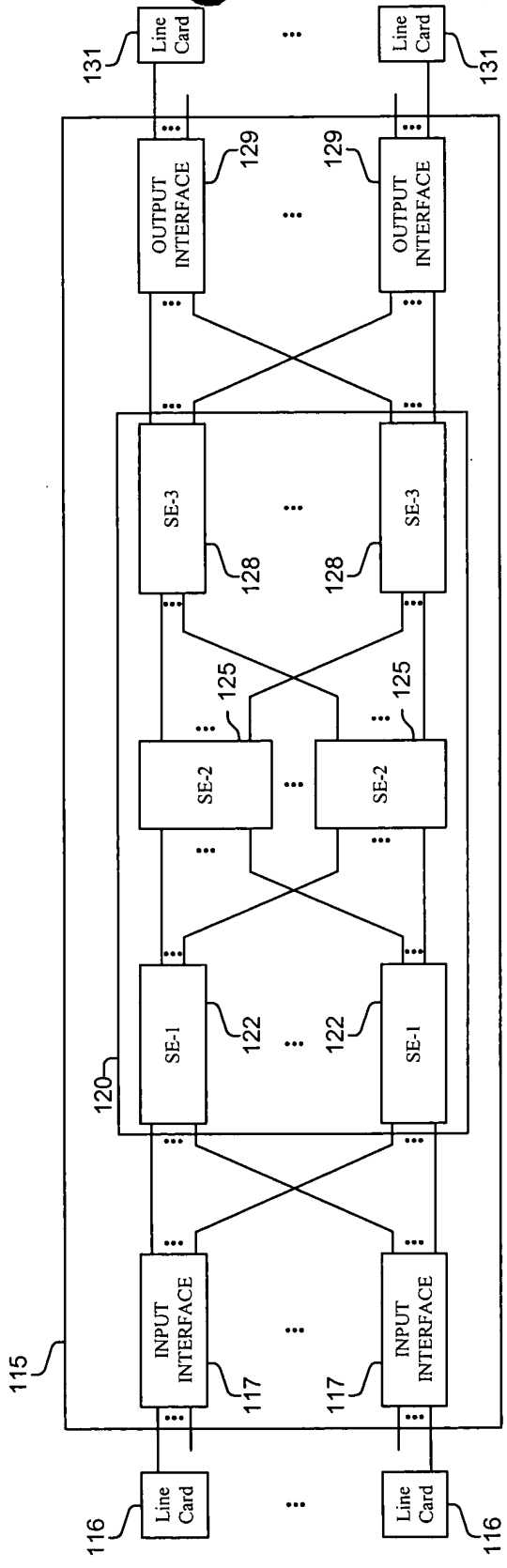


FIGURE 1B

FIG. 1C is a block diagram of a system 140, which includes a plurality of line cards 139, a plurality of input/output interfaces 149, and a plurality of switch elements 142, 145, 148.

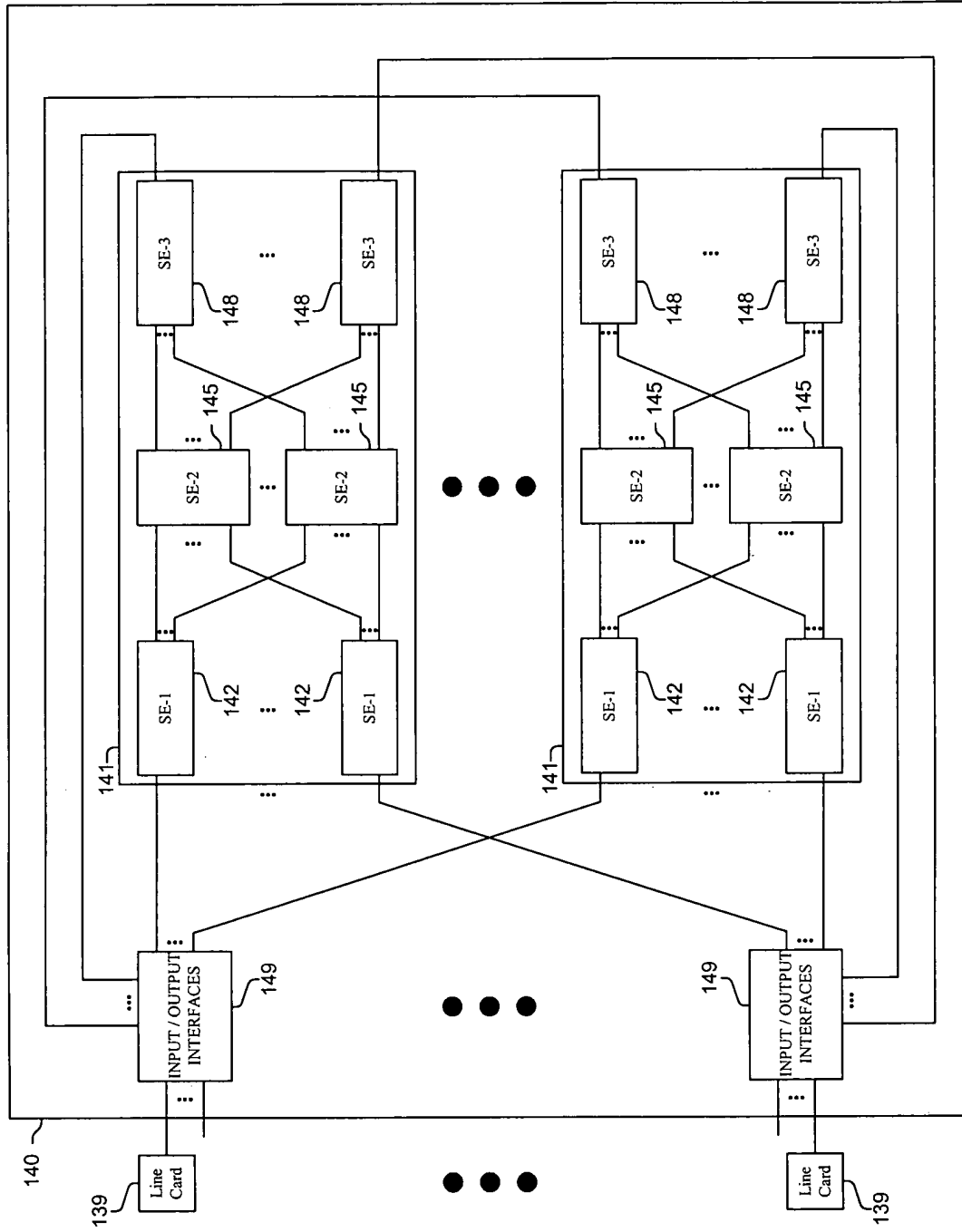


FIGURE 1C

FIG. 1D is a block diagram of a system architecture.

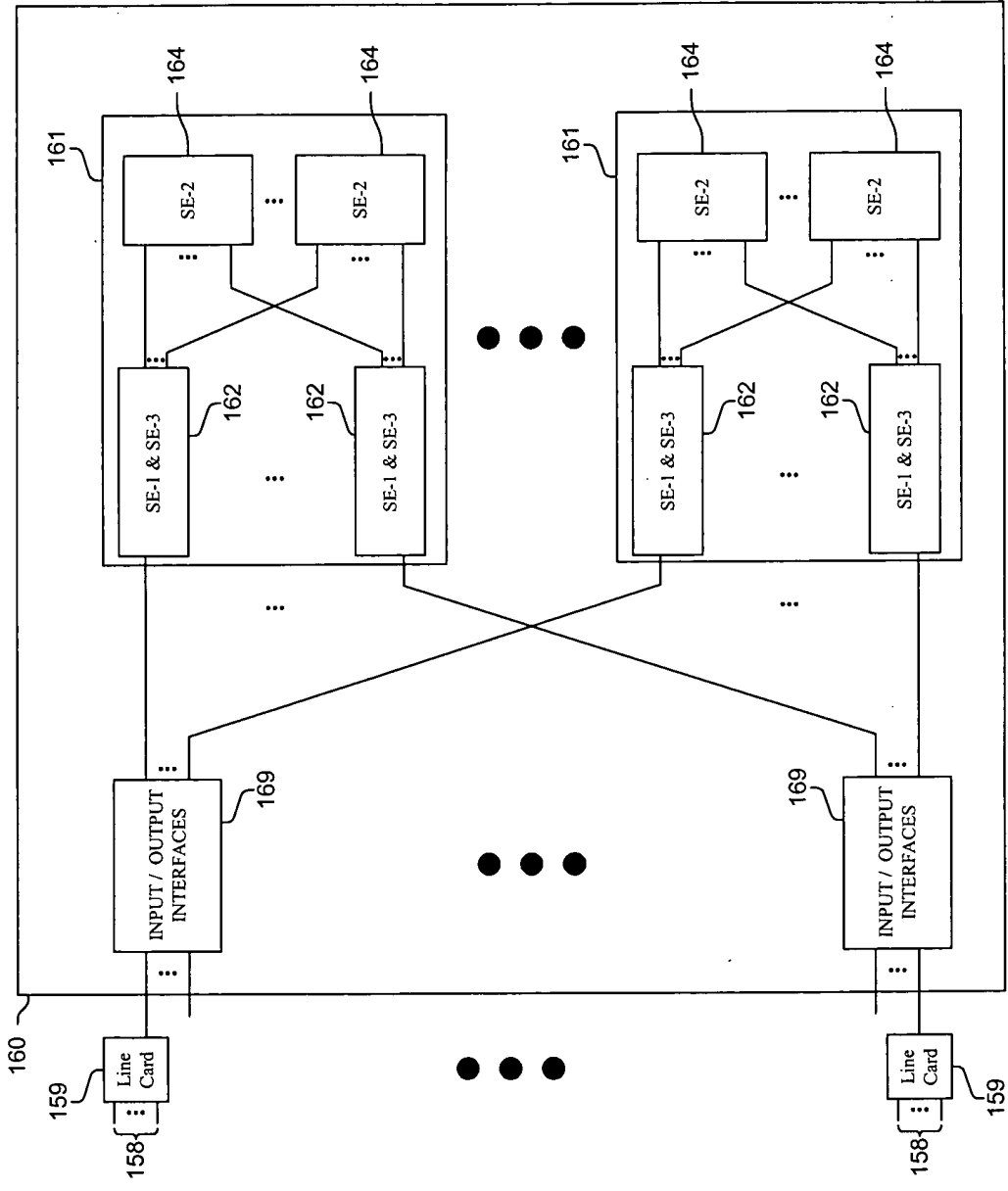


FIGURE 1D

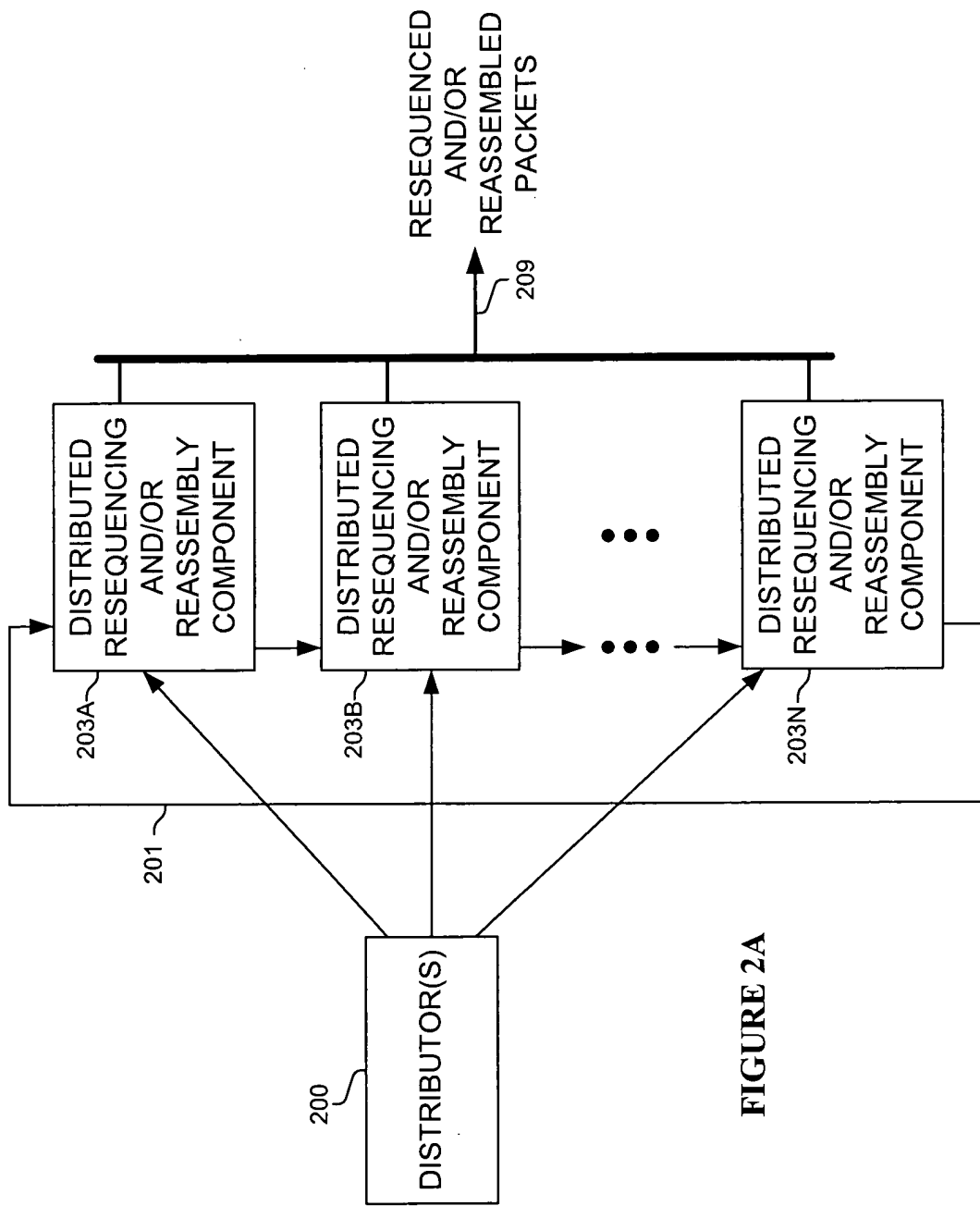


FIGURE 2A

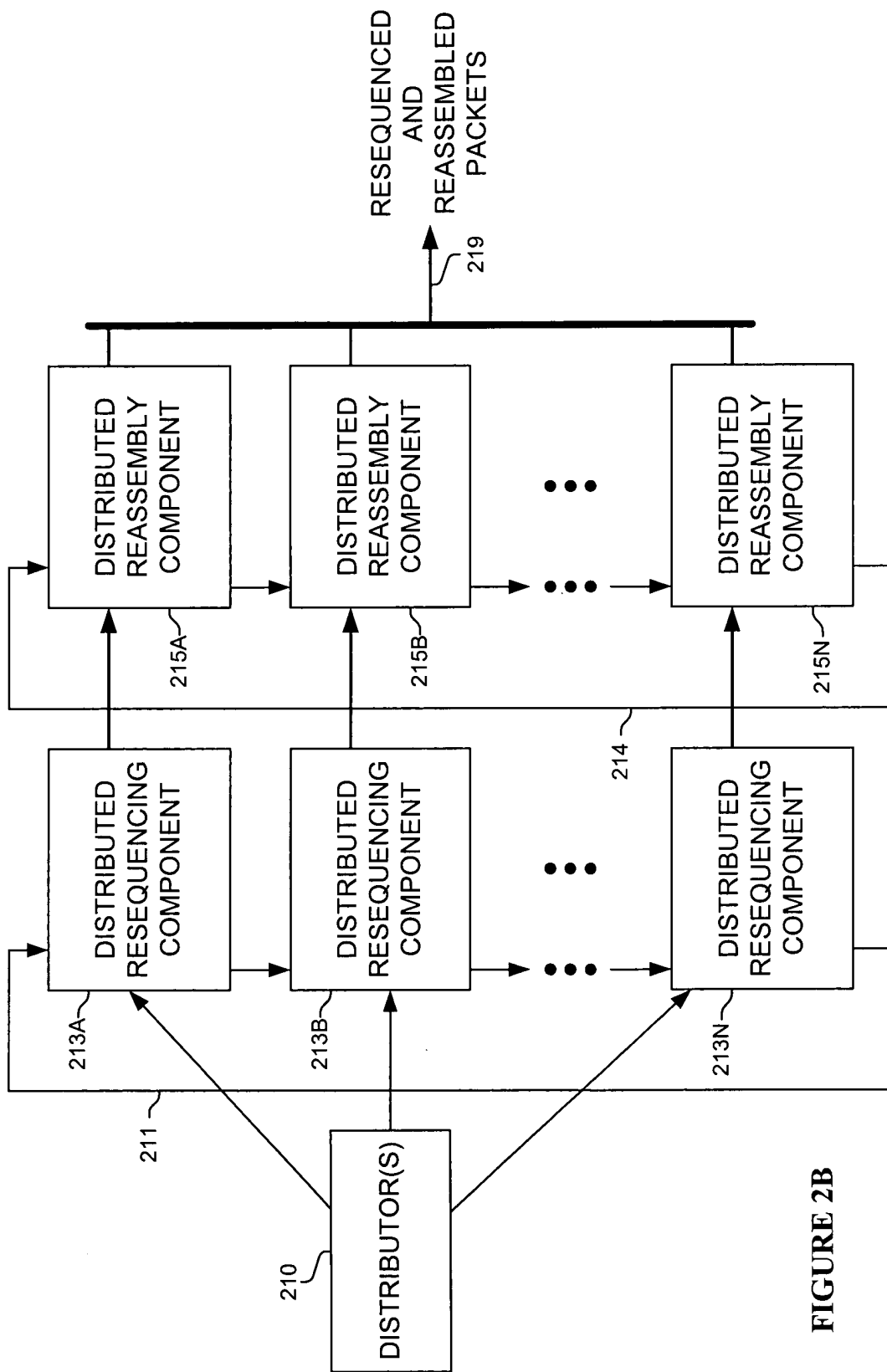


FIGURE 2B

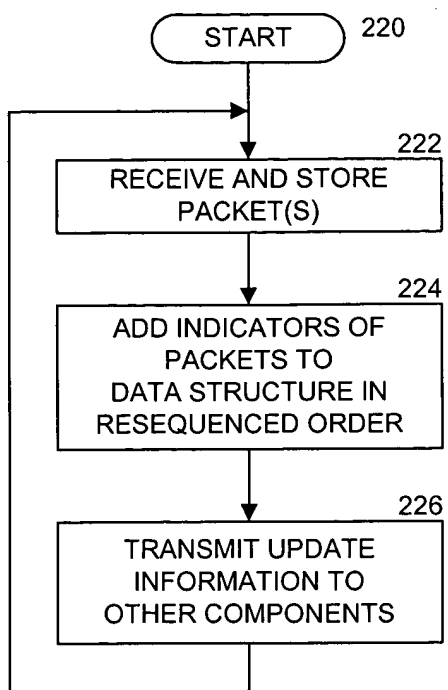


FIGURE 2C

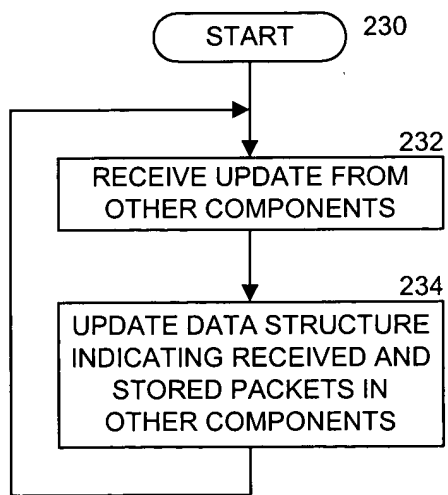


FIGURE 2D

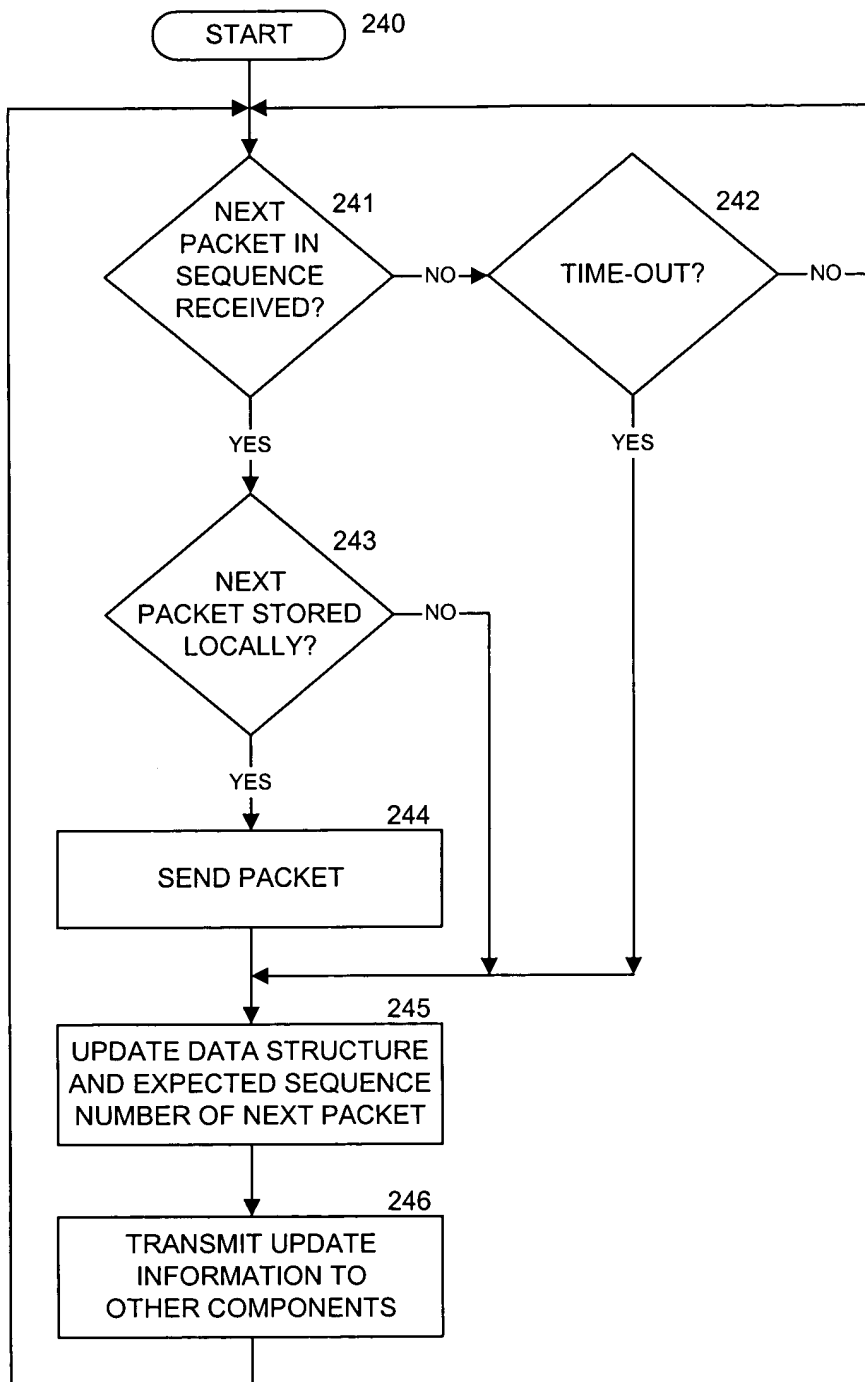


FIGURE 2E

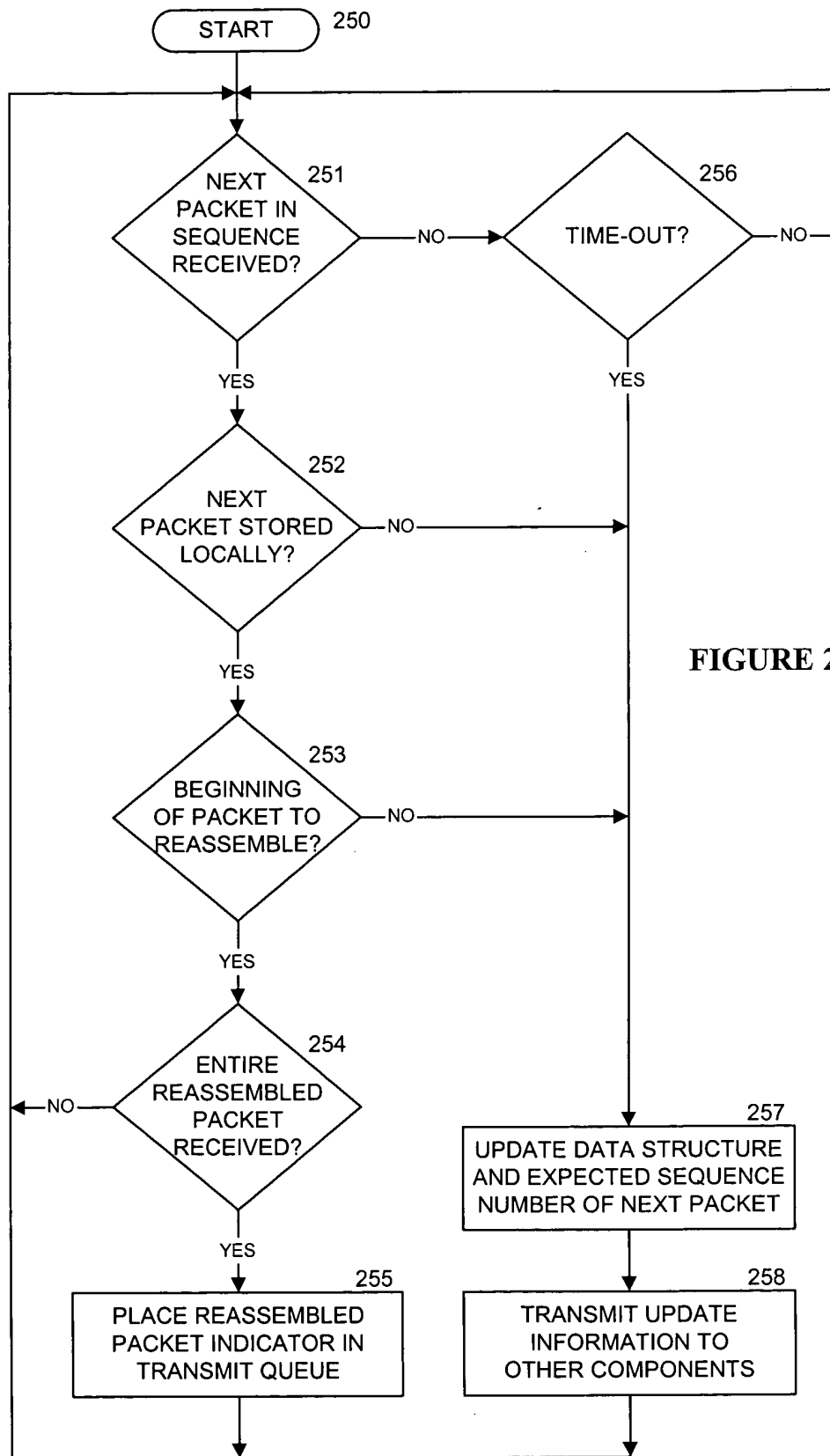


FIGURE 2F

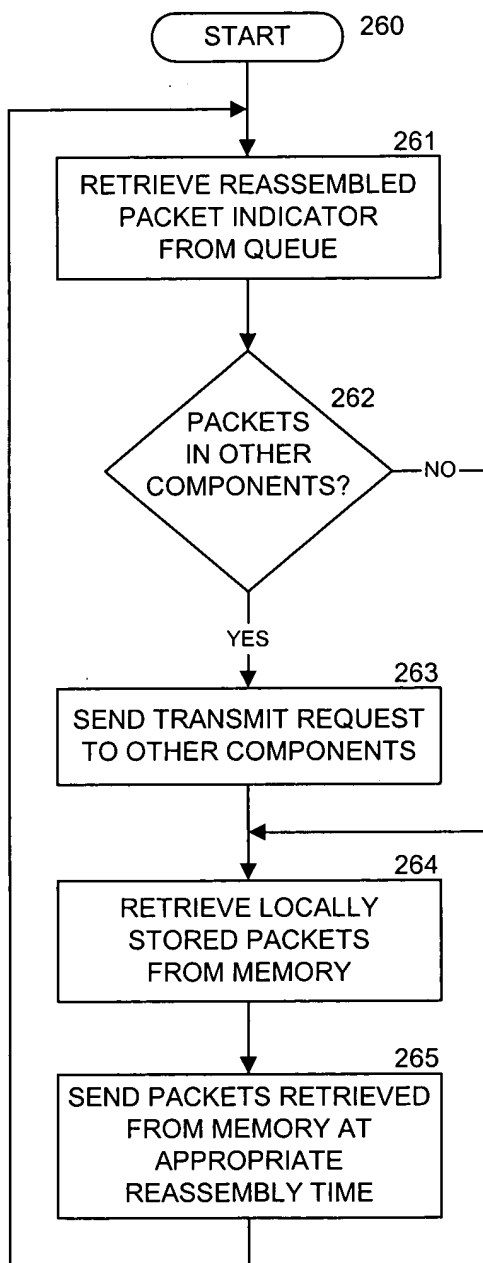


FIGURE 2G

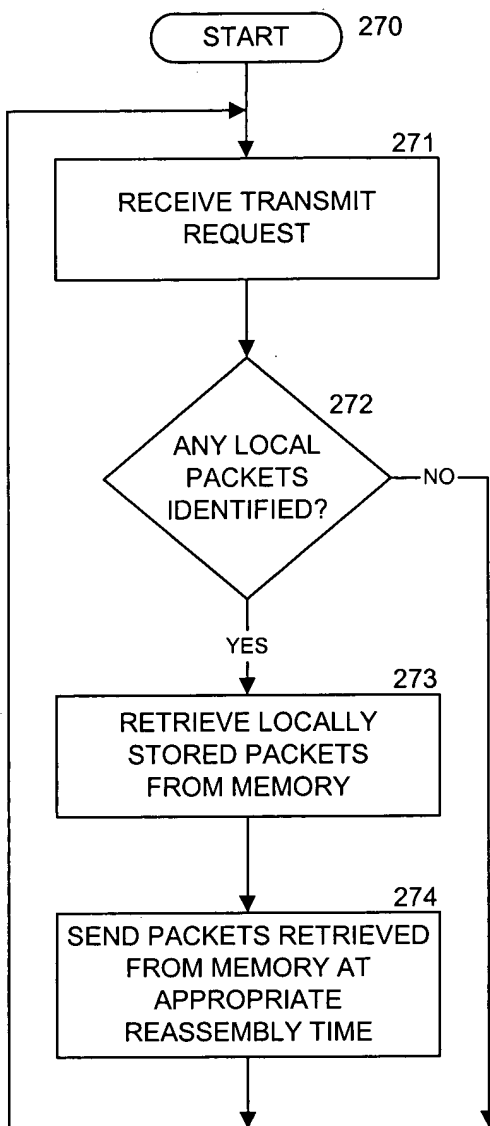
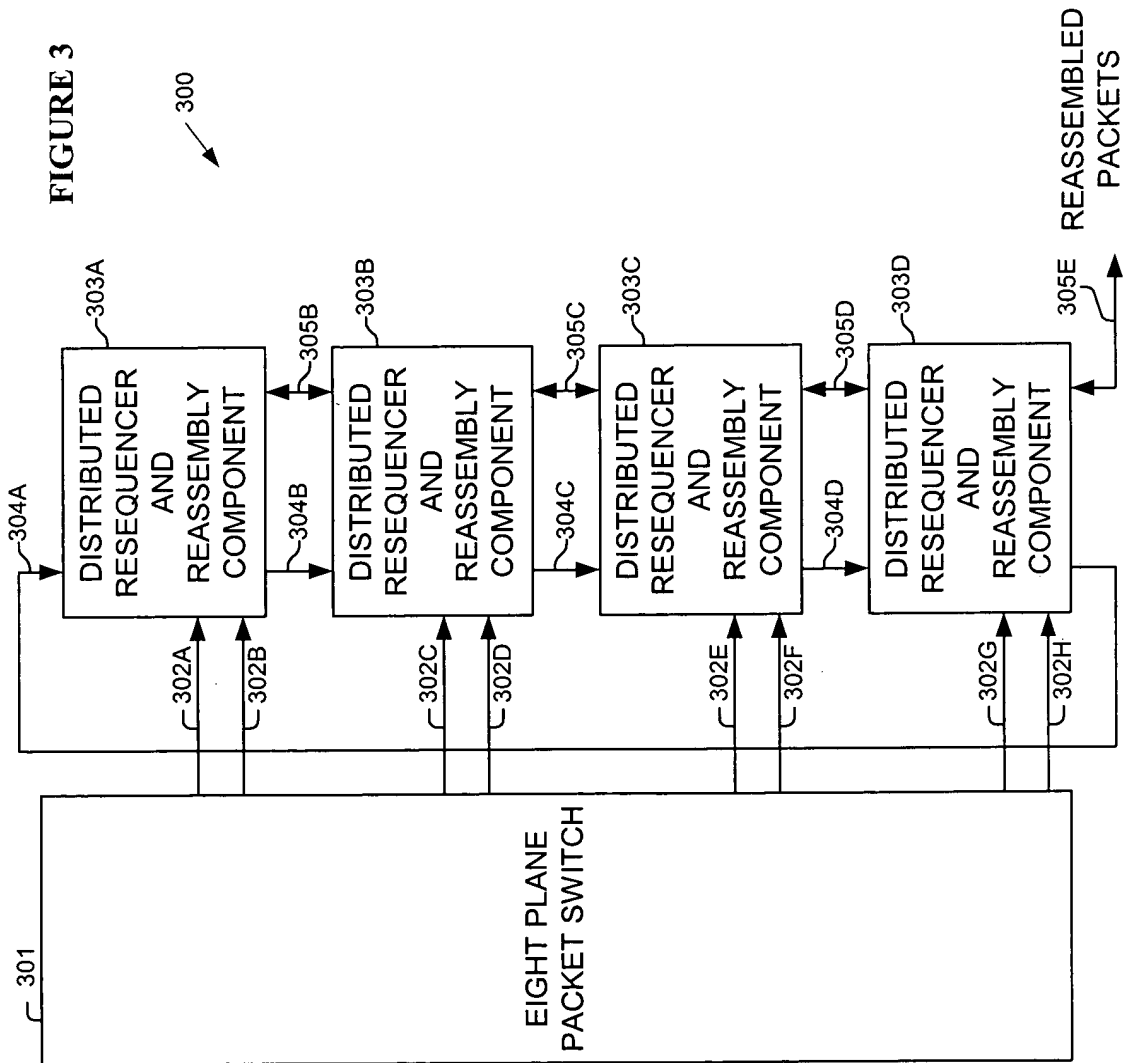


FIGURE 2H



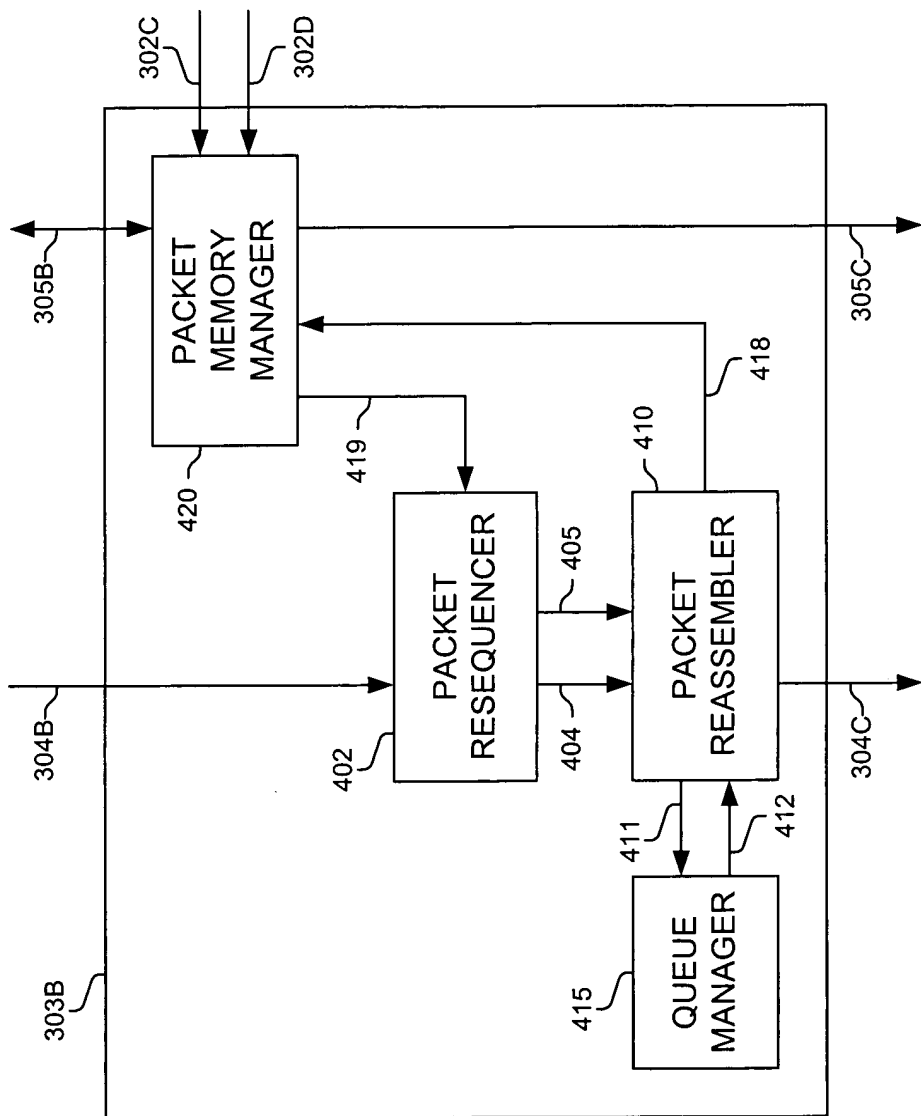


FIGURE 4A

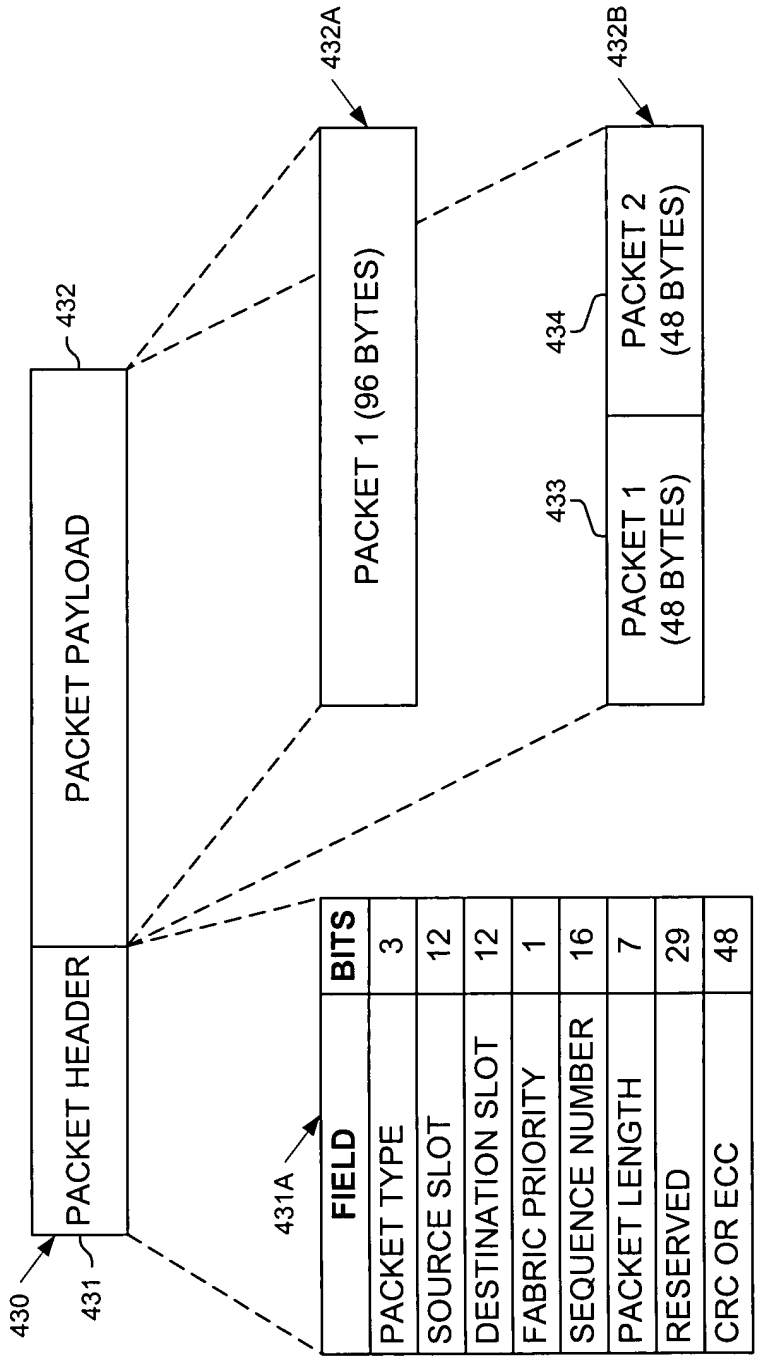
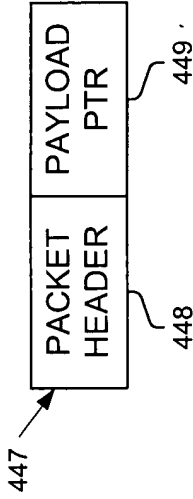
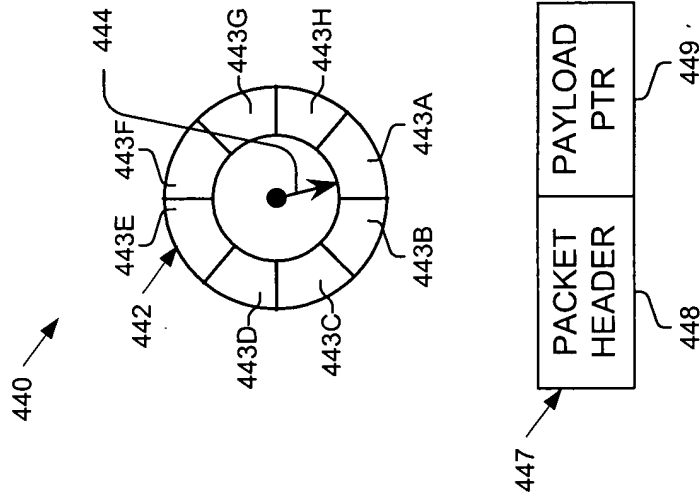
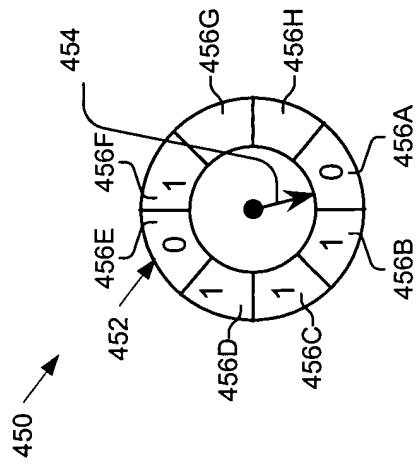


FIGURE 4B



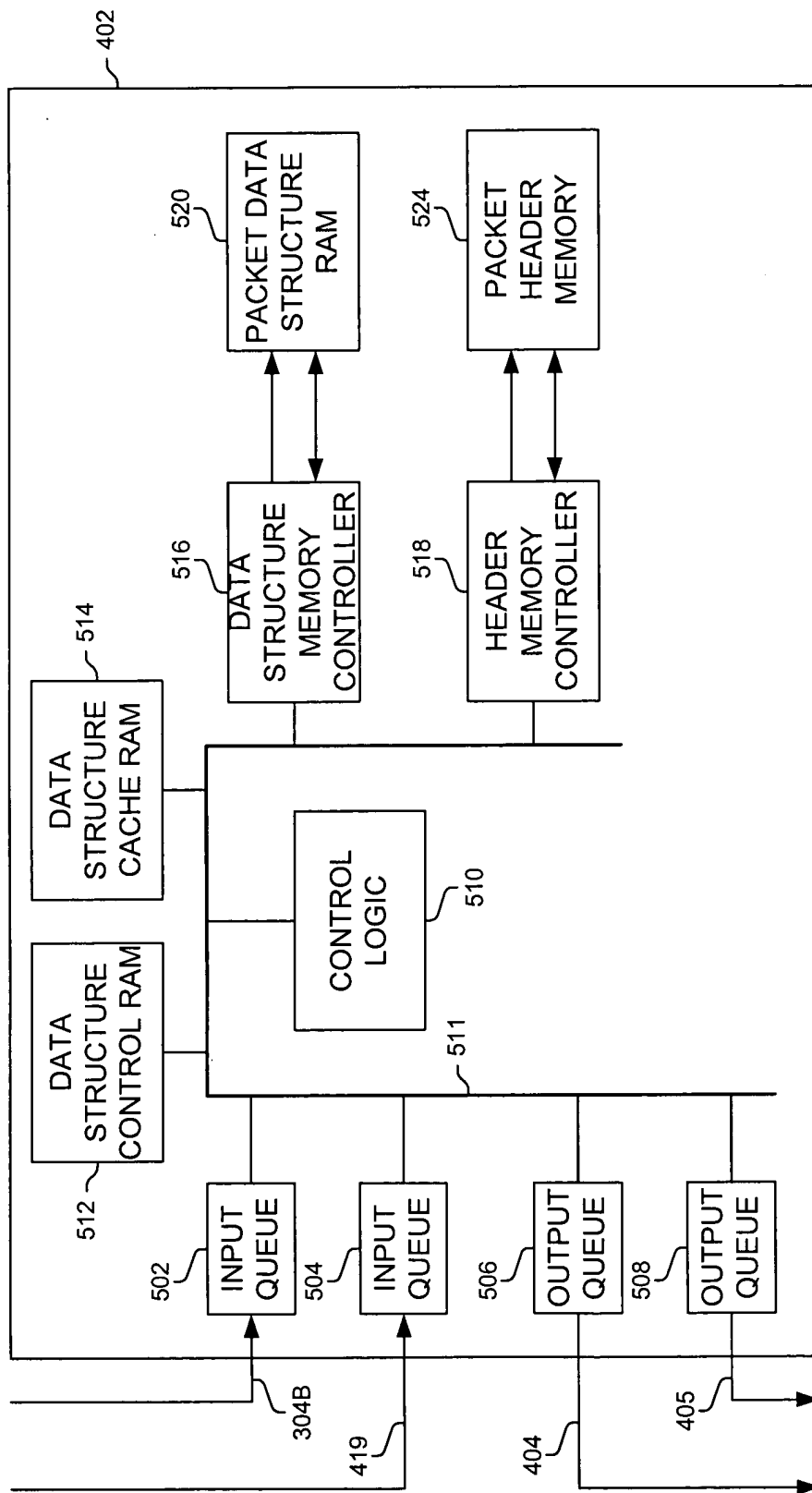
LOCAL DATA
STRUCTURE

FIGURE 4C

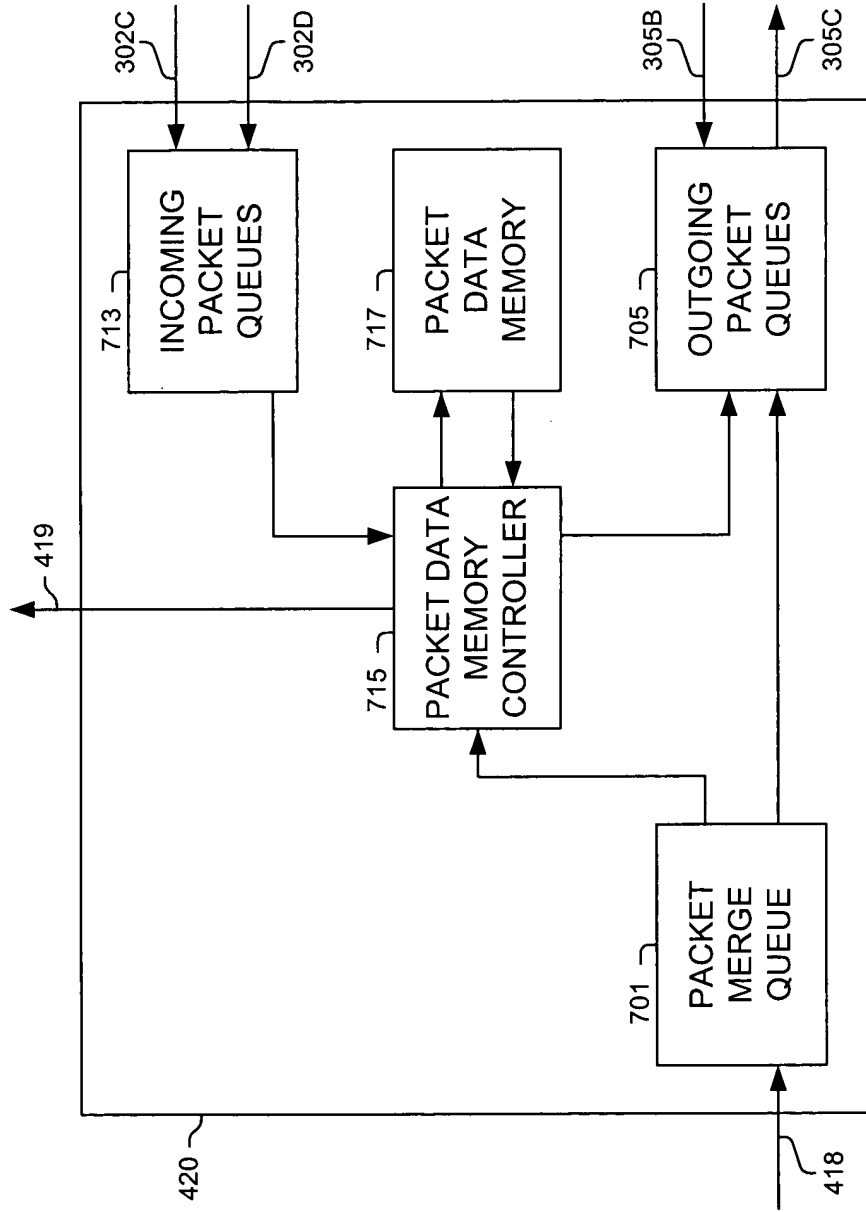


GLOBAL DATA
STRUCTURE

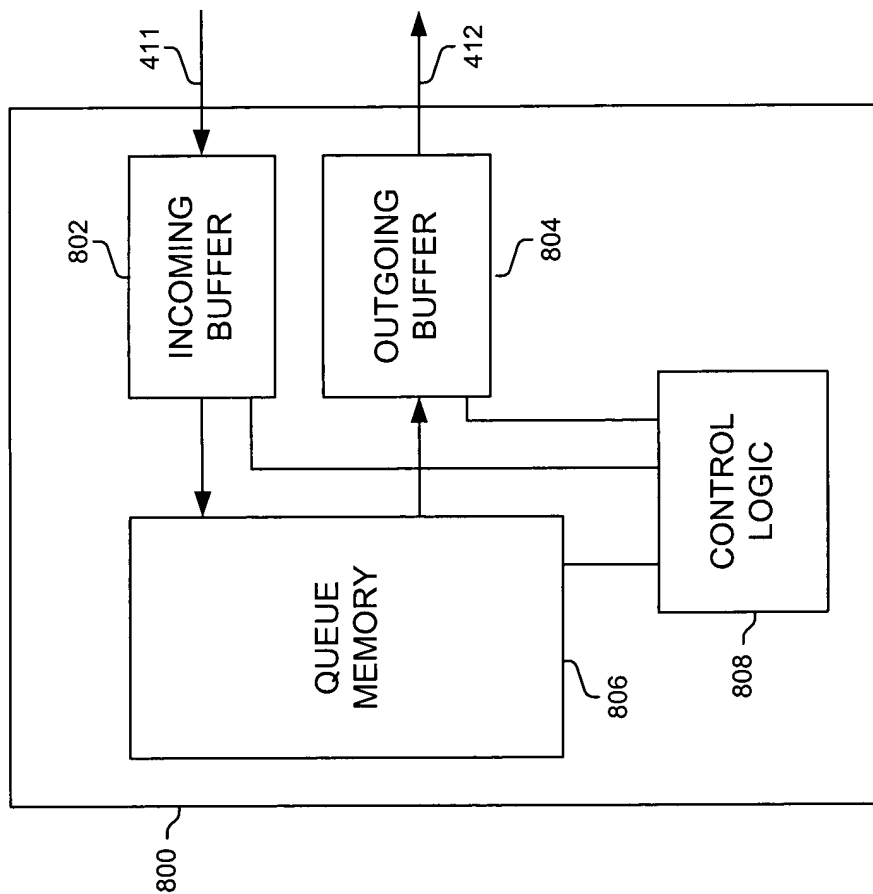
FIGURE 4D



PACKET RESEQUENCER
FIGURE 5



PACKET MEMORY MANAGER
FIGURE 7



QUEUE MANAGER
FIGURE 8